an FET having a gate terminal configured to input a controlled signal and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element and a first capacitor element which are connected to each other in series between a source terminal and a ground terminal of said FET,

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wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit is formed of a reactance component of a gate-to-source impedance and said inductor element, and an inductance value of said inductor element is set in accordance with a frequency of said controlled signal.

IN THE ABSTRACT

Please amend page 17, lines 2-21 as shown in clean form below. A marked-up copy of amended abstract is attached.

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A semiconductor integrated circuit capable of decreasing the amount of signal transmission when an FET is in an OFF state and of improving a variable ratio of the amount of signal transmission, including an inductor element provided between the source terminal and ground terminal of an FET; and Lo input matching circuit provided between the gate terminal and input terminal of the FET; a bias supply circuit connected to the gate terminal of the FET; an RF output matching circuit provided between the drain terminal and output terminal of the FET; a control signal input circuit connected to the drain terminal of the FET; and a bias supply circuit connected to the source terminal of the FET. Since the reactance component of the gate-to-source impedance of the FET series-resonates with the inductor element 1 when the FET is in the OFF state, the amount of signal transmission can be